## CLAIMS

1. A semiconductor memory device, comprising:

a plurality of first memory arrays, a quantity of the first memory arrays being an even number;

a single second memory array comprising a plurality of memory blocks; and

a control circuit associated with each of the first and second memory arrays, the control circuit generating control signals and providing the control signals to the first and second memory arrays such that data is input and output to and from the semiconductor memory device in multiples of nine bits.

2. The semiconductor memory device of claim 1, wherein the control signals are sense amplifier control signals, the sense amplifier control signals selectively activating sense amplifiers in the memory arrays.

3. The semiconductor memory device of claim 1, wherein one of the memory arrays is associated with a quantity of bits of one of one, two, four and eight bits, depending on a data input/output operational configuration of the memory device.

4. The semiconductor memory device of claim 1, wherein, in a by-nine operational configuration, each of two of the first memory arrays is associated with four bits, and the second memory array is associated with a single bit.

5. The semiconductor memory device of claim 1, wherein, in a by-eighteen operational configuration, each of four of the first memory arrays is associated with four bits, and the second memory array is associated with two bits.

6. The semiconductor memory device of claim 1, wherein, in a by-thirty-six operational configuration, each of four of the first memory arrays is associated with eight bits, and the second memory array is associated with four bits.

7. The semiconductor memory device of claim 1, wherein, in a by-seventy-two operational configuration, each of eight of the first memory arrays is associated with eight bits, and the second memory array is associated with eight bits.

8. The semiconductor memory device of claim 1, wherein the memory arrays are arranged in three columns and three rows.

9. The semiconductor memory device of claim 8, further comprising a third memory array redundant to at least one of the first and second memory arrays.

10. The semiconductor memory device of claim 9, wherein the at least one of the first and second memory arrays is divided in half.

11. The semiconductor memory device of claim 8, further comprising a peripheral circuit formed on the semiconductor memory device.

12. The semiconductor memory device of claim 11, wherein the peripheral circuit is formed dividing at least one of the first and second memory arrays.

13. The semiconductor memory device of claim 12, wherein the at least one of the first and second memory arrays is divided in half.

14. The semiconductor memory device of claim 8, further comprising a third memory array redundant to at least one of the first and second memory arrays and a peripheral circuit formed on the semiconductor memory device.

15. The semiconductor memory device of claim 14, wherein the third memory array and the peripheral circuit are formed dividing at least one of the first and second memory arrays.

16. The semiconductor memory device of claim 1, wherein each memory array comprises eight memory blocks and each memory block comprises eight memory segments.

17. The semiconductor memory device of claim 1, wherein all of the plurality of memory arrays have the same input/output operational configuration.

18. The semiconductor memory device of claim 1, wherein the quantity of memory arrays is nine.

19. The semiconductor memory device of claim 1, wherein the quantity of memory arrays is an integer multiple of nine.

20. The semiconductor memory device of claim 1, wherein the memory arrays comprise a plurality of first memory arrays which are selectively activated during a read or write operation and a second memory array which is activated by the control signals during every read or write operation.

21. The semiconductor memory device of claim 1, wherein the memory arrays all have the same memory density.

22. A method of processing data in a semiconductor memory device, comprising:

providing a plurality of first memory arrays, a quantity of the first memory arrays being an even number;

providing a single second memory array comprising a plurality of memory blocks; and

generating control signals and providing the control signals to the first and second

memory arrays such that data is input and output to and from the semiconductor memory device in multiples of nine bits.

23. The method of claim 22, wherein the control signals are sense amplifier control signals, the sense amplifier control signals selectively activating sense amplifiers in the memory arrays.

24. The method of claim 22, wherein one of the memory arrays is associated with a quantity of bits of one of one, two, four and eight bits, depending on a data input/output operational configuration of the memory device.

25. The method of claim 22, wherein, in a by-nine operational configuration, each of two of the first memory arrays is associated with four bits, and the second memory array is associated with a single bit.

26. The method of claim 22, wherein, in a by-eighteen operational configuration, each of four of the first memory arrays is associated with four bits, and the second memory array is associated with two bits.

27. The method of claim 22, wherein, in a by-thirty-six operational configuration, each of four of the first memory arrays is associated with eight bits, and the second memory array is associated with four bits.

28. The method of claim 22, wherein, in a by-seventy-two operational configuration, each of eight of the first memory arrays is associated with eight bits, and the second memory array is associated with eight bits.

29. The method of claim 22, wherein, in a by-nine operational configuration, each of the first memory arrays and the second memory array is associated with one bit of data.

30. The method of claim 22, wherein, in a by-eighteen operational configuration, each of the first memory arrays and the second memory array is associated with two bits of data.

31. The method of claim 22, wherein, in a by-thirty-six operational configuration, each of the first memory arrays and the second memory array is associated with four bits of data.

32. The method of claim 22, wherein each memory array comprises eight memory blocks and each memory block comprises eight memory segments.

33. The method of claim 22, wherein all of the plurality of memory arrays have the same input/output operational configuration.

34. The method of claim 22, wherein the quantity of memory arrays is nine.

35. The method of claim 22, wherein the quantity of memory arrays is an integer multiple of nine.

36. The method of claim 22, wherein the memory arrays comprise a plurality of first memory arrays which are selectively activated during a read or write operation and a second memory array which is activated by the control signals during every read or write operation.